and

(f) etching bared dielectric layer areas.

24. (amended) A method for etching a dielectric layer overlying sn integrated circuit or electronic packaging substrate, comprising:

(a) providing an integrated circuit substrate having a dielectric layer thereof;

(b) over the dielectric layer, depositing a coating layer of an organic antireflective hard mask composition, the composition comprising a resin that comprises one or more inorganic elements selected from Group IIIa, IVa, Va, VIIA, VIII, Ib, IIB, IIIB, IVb, or Vb of the Periodic Table;

(c) depositing a coating of a photoresist composition over the antireflective hard mask composition coating layer;

(d) exposing to patterned radiation and developing the photoresist composition coating layer to form a photoresist relief image over the antireflective hard mask composition;

(e) etching the antireflective hard mask composition to form a relief image thereof; and

(f) etched bared dielectric layer areas.

Please add the following new claims.

30. The method of claim 18 wherein the resin contains Si atoms.

31. The method of claim 18 wherein the photoresist composition is imaged with radiation having a wavelength of about 248 nm, and the antireflective composition resin comprises optionally substituted anthracene groups or optionally substituted napththyl groups.

32. The method of claim 18 wherein the photoresist composition is imaged with radiation having a wavelength of about 193 nm, and the antireflective composition resin